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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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EXAMINER	
NOVACEK, CHRISTY L	
ART UNIT	**PAPER NUMBER**
2822	

DATE MAILED: 09/23/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/619,877	PATON ET AL.	
	Examiner	Art Unit	
	Christy L. Novacek	2822	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *24 June 2004*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-4 and 6-20* is/are rejected.

7)☒ Claim(s) *5* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *6/24/04*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

This office action is in response to the amendment filed June 24, 2004.

Response to Amendment

The limitations added to claim 1 are sufficient to overcome the rejection of claim 1 as being unpatentable over Jang (US 5,654,212) and Chu (US 6,649,492).

The limitations added to claim 17 are sufficient to overcome the rejection of claim 17 as being anticipated by Lustig et al. (US 5,998,807).

Applicant's statement that the Yu (US 6,689,671) reference and the current application are commonly owned is accepted.

Claim Rejections - 35 USC § 103

The text of those sections of Title 35, U.S. Code not included in this action can be found in a prior Office action.

Claims 1-4, 7-10 and 17-20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Zheng et al. (US 6,762,085) in view of Chu et al. (US 6,649,492, previously cited).

Regarding claim 1, Zheng discloses providing a first gate structure (30/3) and a second gate structure (40/3) on a semiconductor substrate (1), wherein the first and second gate structures each include a first spacer (4b) and are provided over first and second areas of the substrate, respectively, providing a first masking layer (10) above the first area, forming first deep source and drain regions (13) in the second area of the substrate, removing the first masking layer, masking the second area of the substrate with a second masking layer (6/15), selectively providing a second spacer (14b) to the first gate structure, and forming second deep source and

drain regions (9) in the first area of the substrate (Fig. 6-10; col. 3, ln. 41 – col. 5, ln. 5). Zheng discloses that the semiconductor substrate is single crystal silicon. Zheng does not disclose that the substrate includes a strained semiconductor layer. Like Zheng, Chu discloses forming a MOSFET on a semiconductor substrate. Chu teaches that it is advantageous to form a MOSFET on a substrate including a strained semiconductor layer because the strained layer increases the electron mobility in the transistors by 95% over transistors made on a substrate of bulk silicon like that of Zheng (col. 4, ln. 49-56). At the time of the invention, it would have been obvious to one of ordinary skill in the art to form the substrate of Zheng such that it includes a strained semiconductor layer because Chu teaches that a strained layer will advantageously increase the electron mobility for MOSFET's such as that of Zheng.

Regarding claim 2, Zheng discloses activating the first and second source/drain regions in an annealing process (col. 5, ln. 17-23).

Regarding claim 3, Zheng discloses that the annealing process is conducted at a temperature of 400-600°C (col. 5, ln. 17-23).

Regarding claim 4, Zheng discloses that the removing of the first masking layer is conducted using dry-etching (plasma ashing) (col. 4, ln. 49-50).

Regarding claim 7, Zheng discloses that the first and second gate structures may include a polysilicon conductor (col. 2, ln. 56-61).

Regarding claim 8, Zheng discloses covering at least a portion of the semiconductor substrate with an insulative layer (2/4a/5a/6/10/14a/15).

Regarding claim 9, Zheng discloses that the second spacers are 200-800 Angstroms wide (col. 4, ln. 49-52).

Regarding claim 10, Zheng discloses that the second source/drain regions (in the first area of the substrate) include Arsenic (col. 3, ln. 64 – col. 4, ln. 5).

Regarding claim 17, Zheng discloses forming a plurality of gate structures on a top surface of a silicon layer/substrate, covering a first set of gate structures, forming deep source/drain regions on each side of a second set of gate structures, uncovering the first set of gate structures, covering the second set of gate structures, selectively providing spacers for the first set of gate structures, and forming deep source/drain regions on each side of the first set of gate structures. Zheng does not disclose that the transistors are provided on a top surface of a strained silicon layer. For the reasons stated above in reference to claim 1, at the time of the invention, it would have been obvious to one of ordinary skill in the art to form the substrate of Zheng such that it has a strained semiconductor layer.

Regarding claim 18, Zheng discloses annealing the entire semiconductor device, including the substrate after the step of selectively providing spacers to the first set of gate structures.

Regarding claim 19, Chu discloses that the strained silicon layer should be provided above a silicon germanium layer.

Regarding claim 20, Zheng discloses that the deep source/drain regions are provided by ion implantation.

Claims 11 and 14-16 are rejected under 35 U.S.C. 103(a) as being unpatentable over Haken (US 5,141,890, previously cited) in view of Chu et al. (US 6,649,492, previously cited).

Regarding claim 11, Haken discloses selectively providing deep source/drain regions for a first group of transistors, selectively providing offset spacers for a second, different, group of

transistors, and selectively providing source/drain regions for the second group of transistors. Haken does not disclose providing the first and second groups of transistors on a top surface of a strained semiconductor layer. Like Haken, Chu discloses forming a MOSFET on a semiconductor substrate. Chu teaches that it is advantageous to form a MOSFET on a substrate including a strained semiconductor layer because the strained layer increases the electron mobility in the transistors by 95% over transistors made on a substrate of bulk silicon like that of Haken (col. 4, ln. 49-56). At the time of the invention, it would have been obvious to one of ordinary skill in the art to form the substrate of Haken such that it includes a strained semiconductor layer because Chu teaches that a strained layer will advantageously increase the electron mobility for MOSFET's such as that of Haken.

Regarding claim 14, Chu discloses that the strained semiconductor layer should include silicon.

Regarding claim 15, Chu discloses that the silicon should be above a silicon/germanium layer.

Regarding claim 16, Haken discloses that a 3000 Angstrom thick oxide is used for forming the offset spacers on a 5000 Angstrom thick polysilicon layer. The width of the spacers is a results effective variable as it determines the channel length and must shrink as channel length decreases. Official notice is taken that the channel length of CMOS devices generally shrinks with each new generation of devices and that this reduction in size is desirable. Accordingly, at the time of the invention, one of ordinary skill in the art would have been motivated to use thinner spacers in order to keep the channel length in line with the general trend in device fabrication.

Claim 12 is rejected under 35 U.S.C. 103(a) as being unpatentable over Haken and Chu as applied to claim 11 above, and further in view of Sitaram et al. (US 5,384,285, previously cited).

Regarding claim 12, Haken does not disclose forming a silicide layer above the source/drain regions for the first and second groups of transistors. Like Haken, Sitaram teaches forming a MOSFET. Sitaram teaches that it is beneficial to form silicide over the source/drain regions of these transistors in order to decrease contact resistance. At the time of the invention, it would have been obvious to one of ordinary skill in the art to provide a silicide layer above the source/drain regions for the transistors of Haken because Sitaram teaches that it is beneficial to do so.

Claim 13 is rejected under 35 U.S.C. 103(a) as being unpatentable over Haken and Chu and Sitaram as applied to claim 12 above, and further in view of Blair et al. (US 5,998,873, previously cited).

Regarding claim 13, Haken does not disclose forming a silicon oxide layer over a silicide layer on the source/drain regions. Like Haken, Blair discloses forming a MOSFET. Blair discloses that typical integrated circuits include metal interconnect structures that serve a variety of purposes, such as carrying electrical signals between individual device elements in the IC, supplying power, and providing a connection to ground and to external apparatus (col. 1, ln. 15-20). Blair teaches that these metal interconnects are conventionally isolated by interlevel dielectric layers of silicon oxide. At the time of the invention, it would have been obvious to one of ordinary skill in the art to form an interlevel silicon oxide dielectric layer over the silicide

layer of Haken because, as Blair recites, it is conventional in the art to form such layers over the surface of an IC device in order to provide for metal interconnects which supply power and interconnections to the devices of the IC component.

Claims 1, 7, 8 and 17 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kim et al. (US 5,291,052) in view of Chu et al. (US 6,649,492, previously cited).

Regarding claim 1, Kim discloses providing a first gate structure (6) and a second gate structure (6) on a semiconductor substrate (1), wherein the first and second gate structures each include a first spacer (8a) and are provided over first and second areas of the substrate, respectively, providing a first masking layer (11/13) above the first area, forming first deep source and drain regions (9) in the second area of the substrate, removing the first masking layer, masking the second area of the substrate with a second masking layer (16), selectively providing a second spacer (15a) to the first gate structure, and forming second deep source and drain regions (10) in the first area of the substrate (Fig. 3D-3G; col. 5, ln. 30 – col. 6, ln. 8). Kim discloses that the semiconductor substrate is silicon. Kim does not disclose that the substrate includes a strained semiconductor layer. Like Kim, Chu discloses forming a MOSFET on a semiconductor substrate. Chu teaches that it is advantageous to form a MOSFET on a substrate including a strained semiconductor layer because the strained layer increases the electron mobility in the transistors by 95% over transistors made on a substrate of bulk silicon like that of Kim (col. 4, ln. 49-56). At the time of the invention, it would have been obvious to one of ordinary skill in the art to form the substrate of Kim such that it includes a strained semiconductor layer because Chu teaches that a strained layer will advantageously increase the electron mobility for MOSFET's such as that of Kim.

Regarding claim 7, Kim discloses that the first and second gate structures include a polysilicon conductor.

Regarding claim 8, Kim discloses covering at least a portion of the semiconductor substrate with an insulative layer (4/5/11/8/13/15/16).

Regarding claim 17, Kim discloses forming a plurality of gate structures on a top surface of a silicon layer/substrate, covering a first set of gate structures, forming deep source/drain regions on each side of a second set of gate structures, uncovering the first set of gate structures, covering the second set of gate structures, selectively providing spacers for the first set of gate structures, and forming deep source/drain regions on each side of the first set of gate structures. Kim does not disclose that the transistors are provided on a top surface of a strained silicon layer. For the reasons stated above in reference to claim 1, at the time of the invention, it would have been obvious to one of ordinary skill in the art to form the substrate of Kim such that it has a strained semiconductor layer.

Claim 6 is rejected under 35 U.S.C. 103(a) as being unpatentable over Kim and Chu as applied to claim 1 above, and further in view of Sitaram et al. (US 5,384,285, previously cited).

Regarding claim 6, Kim does not disclose forming a silicide layer above the source/drain regions of the first and second transistors. Like Kim, Sitaram teaches forming a MOSFET. Sitaram teaches that it is beneficial to form silicide over the source/drain regions of these transistors in order to decrease contact resistance. At the time of the invention, it would have been obvious to one of ordinary skill in the art to provide a silicide layer above the source/drain regions for the transistors of Kim because Sitaram teaches that it is beneficial to do so.

Response to Arguments

Applicant's arguments filed June 24, 2004 have been fully considered.

The Examiner agrees with Applicant's argument that the limitations added to claims 1 and 17 are sufficient to overcome the previously made rejections of those claims. Accordingly, those rejections have been withdrawn.

Regarding the rejection of claim 11 as being unpatentable over Haken in view of Chu, Applicant argues that there is not sufficient motivation to combine the Chu and Haken references. The motivation to combine these references can be found in the Chu reference itself, which specifically teaches that it is beneficial to form an IC substrate such that it has a strained top surface layer in order that electron mobility may be enhanced over that of the traditional bulk silicon (non-strained) substrate. Therefore, the rejection of claim 11 as being unpatentable over Haken in view of Chu is maintained.

Allowable Subject Matter

Claim 5 is objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

The primary reason for the indication of the allowable subject matter of claim 5 is the inclusion therein, in combination as currently claimed, of the limitation of forming both the first and second spacers of nitride. This limitation is found in claim 5 and is neither disclosed nor taught by the prior art of record, alone or in combination.

Conclusion

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Christy L. Novacek whose telephone number is (571) 272-1839. The examiner can normally be reached on Monday-Thursday and alternate Fridays 7:30 - 5:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Amir Zarabian can be reached on (571) 272-1852. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

CLN
September 20, 2004

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